What is Claimed Is:

1. In a network switching system having an ingress processor for receiving incoming frames from a port of a network, and an egress processor having a port through which said frames are delivered, a method for enhancing processor speed by the egress processor comprising:

forming at said ingress processor a header for each frame destined for said egress processor having data for identifying a beginning of a processing sequence for said egress processor; and

decoding said data in said header in a hardware frame classifier into a starting address for said egress processor.

2. The method for enhancing processing according to claim 1 wherein said frame header includes control information for said egress processor which distinguish said frames as being multicast or unicast.

3. The method for enhancing processing according to claim 1 wherein said step of decoding said instructions include indexing an address table in said hardware frame classifier; and

executing processing from a starting address space identified by said table of said hardware classifier.

4. The method for enhancing processing according to claim 3 wherein processing of said frame begins at a process execution level determined from a port configuration entry of the interface of the port said frame was received if a configuration bit of said egress processor indicates said hardware classifier has been disabled.

5. The method for enhancing processing according to claim 1 wherein said egress processor creates multiple frames for multiple output ports when said frame header contains multicast data.

6. The method for enhancing processing according to claim 1 wherein a parameter is encoded into a field of said frame header by said ingress processor which is read by an instruction executed by said egress processor.

7. The method for enhancing processing according to claim 3 wherein said data is located in two fields, the first of which identifies the number of bytes in a second field containing parameters for execution by said egress processor.

8. A network switch for enhancing execution of frame classification information comprising:

an ingress processor for parsing and recovering parameters from said frame and recovering the identity of said frame;

said processor being further programmed to create a header for an intra-switch frame identifying said received frame and a level of processing of said received frame;

an egress processor for receiving said intra-switch frame and for creating a frame for passing to one or more output ports, said processor being programmed to:

execute instructions which follow a starting address for completing processing of said frame; and

forward said processed frame to an output port based on said processing of said frame; and

a hardware frame classifier for determining from said intra-switch frame header said starting address of said instructions which are to be processed.

9. The network switch according to claim 8 wherein said hardware frame classifier includes an address table which decodes frame header extension values and variable frame extension values which point to said egress processor starting address location.

10. The network switch according to claim 8 wherein said header includes a field which identifies the number of bytes in a variable length field which contain parameters determined by said ingress processor.

11. The network switch according to claim 8 wherein said frame header includes a field to identify said received frame as being a multicast frame.

12. The network switch according to claim 8 wherein said frame header data is stored in fixed length fields which have a length determined by a length field in said header.

13. In a network switch which receives frames of data on a set of input ports and delivers said frames to an output port, a method for improving frame processing time comprising:

partially processing a received frame in an ingress processor which parses said frame parameters and prepares an intraswitch frame for delivery to an egress processor associated with said output port; said ingress processor creating a header for said intraswitch frame having a data for identifying parameters computed by said ingress processor and for identifying a starting address for said egress processor; and

completing processing of said frame in an egress processor which receives said intraswitch frame and passes said processed frame to an output port, said egress processor completing processing from program instructions which have a starting address defined by said header data and from parameters computed by said ingress processor, whereby processing performed by said ingress

processor is not unnecessarily performed by said egress processor.

14. The method for improving frame processing according to claim 13 wherein said ingress processor encodes in said header data representing a level of processing completed by said ingress processor.

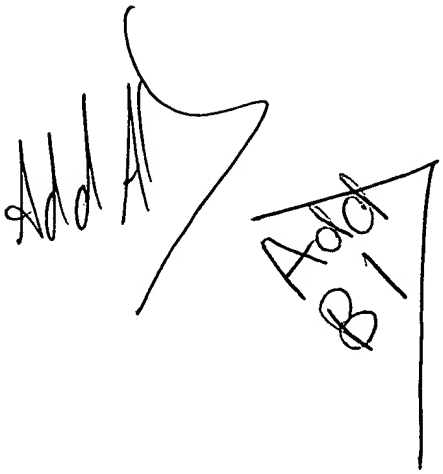
15. The method for improving frame processing according to claim 13 wherein said ingress processor creates multiple fields in said header for indicating the type of frame received, and for indicating the level of processing completed by said ingress processor.

16. The method for improving frame processing according to claim 13 wherein a hardware classifier identifies said starting address from said identifying data in said header.

17. The method for improving frame processing according to claim 16 wherein said hardware classifier locates said address from a table which is indexed by said recovered data.

18. The method for improving frame processing according to claim 13 wherein said egress processor is programmed to detect a multicast bit contained in said frame header which identifies said

A1 Cont'4 frame as being destined to multiple ports.



DOCKET ALARM